EE 330
Lecture 10

IC Fabrication Technology

- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Planarization
- Contacts, Interconnect, and Metallization

Exam 1 Schedule

Exam 1 will be given on Friday September 23

Format: Open-Book, Open Notes

Exam will be posted at 9:00 a.m. on the class WEB site and will be due at 1:00 p.m. as a .pdf upload on CANVAS

It will be structured to be a 50-minute closed-book closed-notes exam but administered as an open-book, open-notes exam with a 4 hour open interval so reserving the normal lecture period for taking the exam should provide adequate time

Honor System Expected

It is expected that this exam be an individual effort and that students should not have input in **any form** from **anyone else** during the 4-hour open interval of the exam except from the course instructor who will be responding to email messages from 11:00 a.m. to 1:00 p.m. on the date of the exam.

Special Accommodations

For anyone with approved special accommodations, the 4-hour open interval should cover extra time allocations but if for any reason this does not meet special accommodation expectations, please contact the instructor by Monday Sept. 14 if alternative accommodations are requested.

Photolithographic Process

- Photoresist
  - Viscous Liquid
  - Uniform Application Critical (spinner)
  - Baked to harden
  - Approx 1u thick
  - Non-Selective
  - Types
    - Negative – unexposed material removed when developed
    - Positive-exposed material removed when developed
    - Thickness about 450nm in 90nm process (ITRS 2007 Litho)
- Exposure
  - Projection through reticle with stepper (scanners becoming popular)
  - Alignment is critical !!
  - E-Bean Exposures
    - Eliminate need fro reticle
    - Capacity very small

Stepper: Optics fixed, wafer steps in fixed increments
Scanner: Wafer steps in fixed increments and during exposure both optics and wafer are moved to increase effective reticle size

Review from Last Time

Deposition

- Application of something to the surface of the silicon wafer or substrate
  - Layers 15A to 20u thick
- Methods
  - Physical Vapor Deposition (nonselective)
    - Evaporation/Condensation
    - Sputtering (better host integrity)
  - Chemical Vapor Deposition (nonselective)
    - Reaction of 2 or more gases with solid precipitate
    - Reduction by heating creates solid precipitate (pyrolytic)
  - Screening (selective)
    - For thick films
    - Low Tech, not widely used today

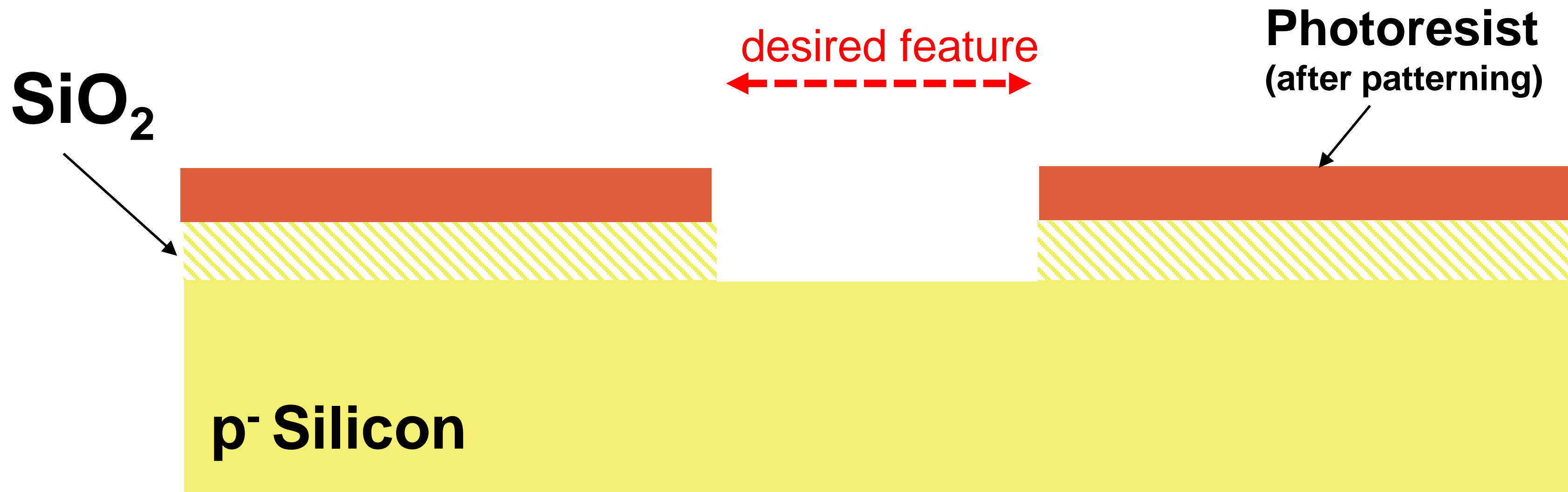
Review from Last Time

Masking

Mask Features

Review from Last Time

Etching



Desired Physical Features

Note: Vertical Dimensions in silicon generally orders of magnitude smaller than lateral dimensions so different vertical and lateral scales will be used in this discussion. Vertical dimensions of photoresist which is applied on top of wafer is about ½ order of magnitude larger than lateral dimensions

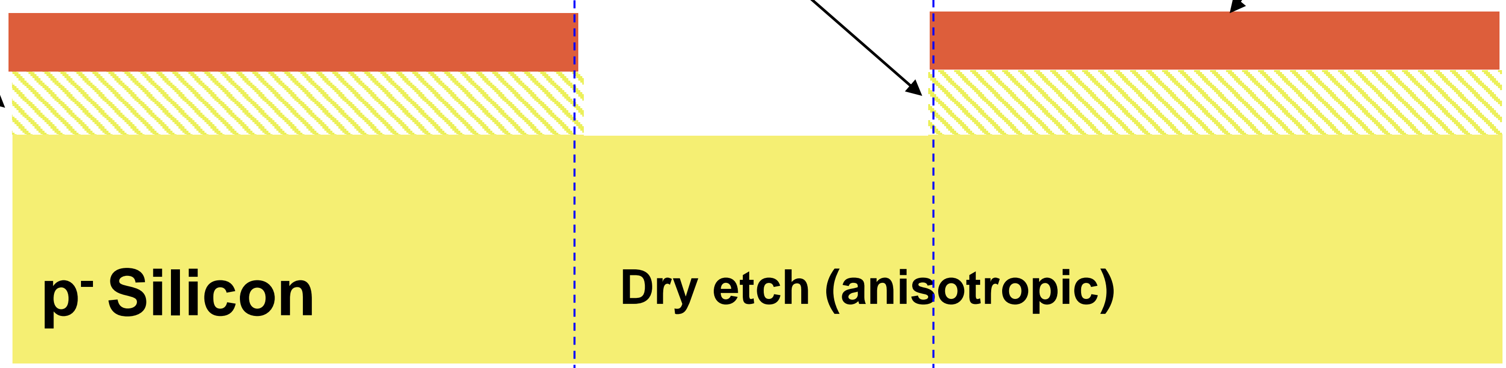
Review from Last Time

Etching (limited by photolitghographic process)

SiO_2

Dry etch (anisotropic)

Photoresist



Consider neg photoresist

Over Exposed

Correctly Developed

Over Developed

Under Developed

Under Exposed

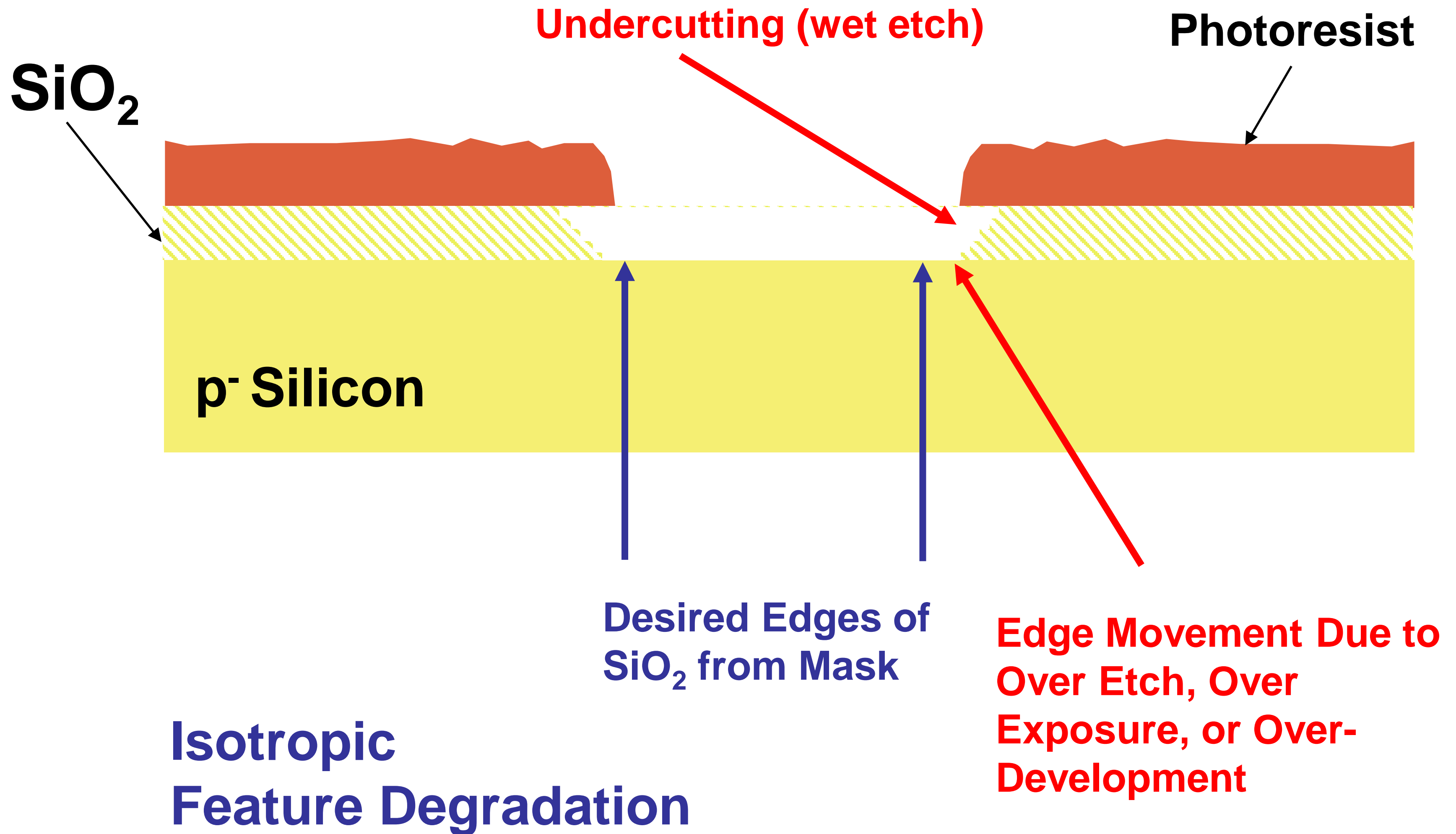
Correctly Developed

Over Developed

Under Developed

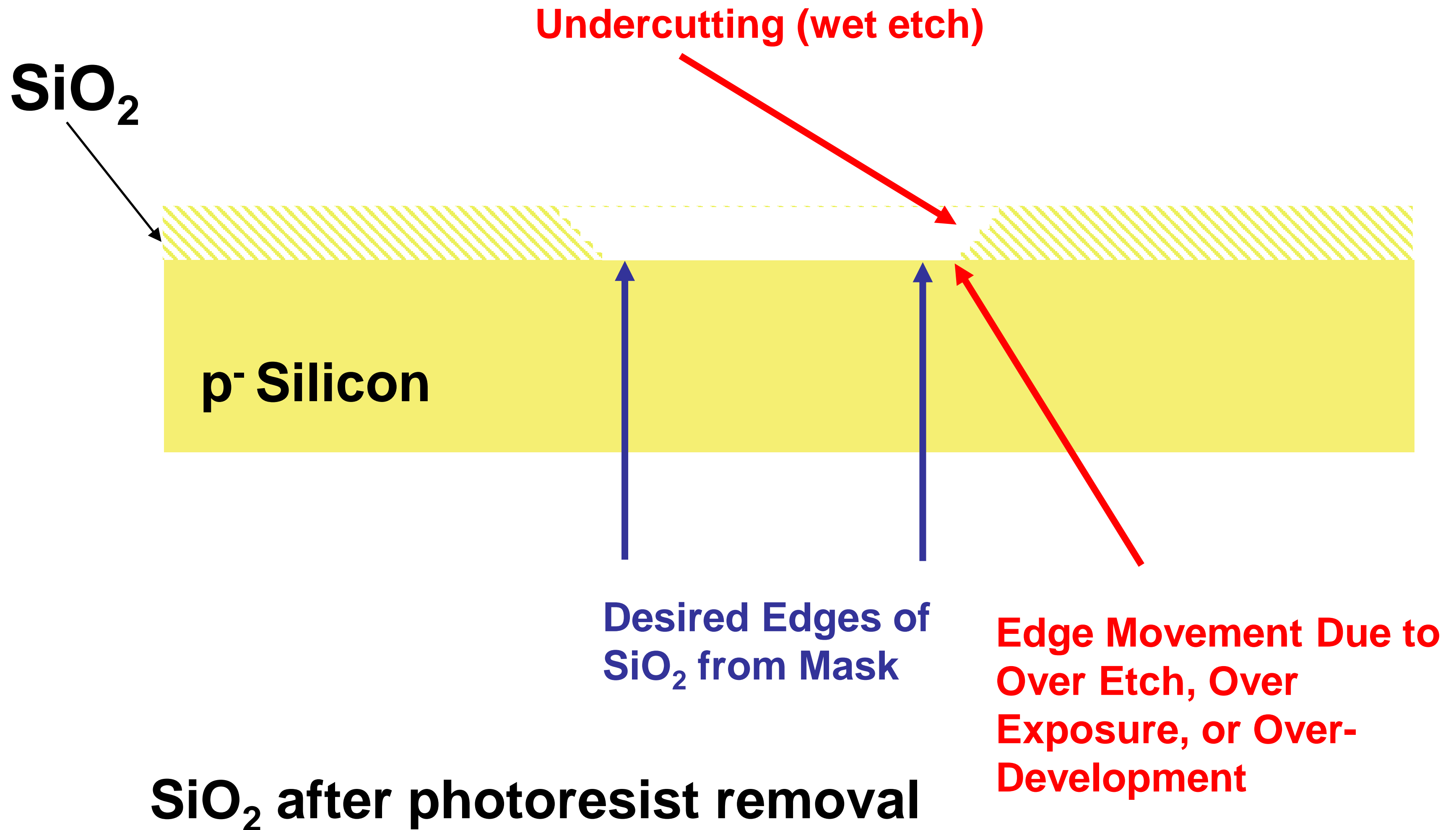
Review from Last Time

Etching



Review from Last Time

Etching



SiO_2 after photoresist removal

IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Ion Implantation
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
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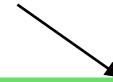
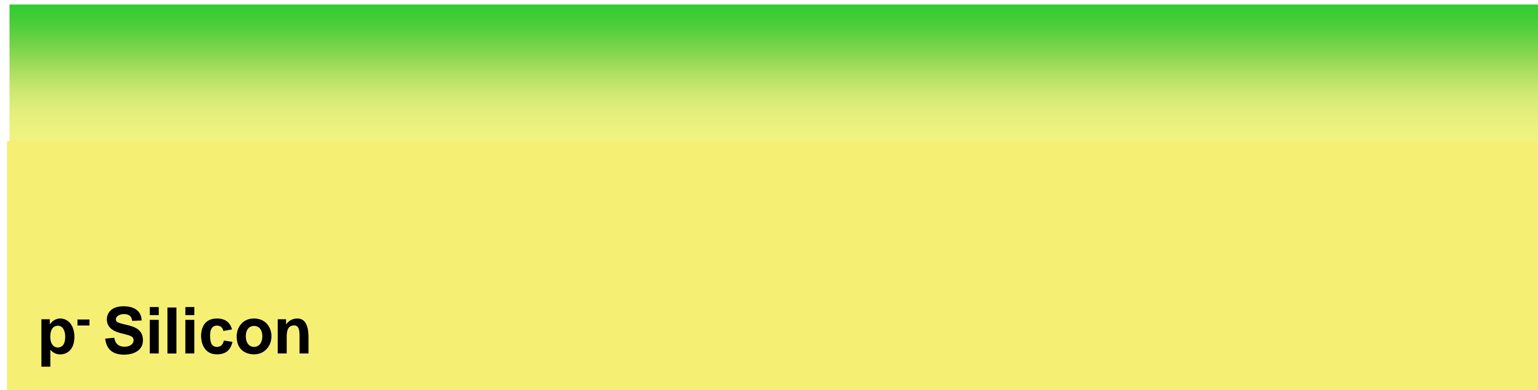
Diffusion

- Controlled Migration of Impurities
  - Time and Temperature Dependent
  - Both vertical and lateral diffusion occurs
  - Crystal orientation affects diffusion rates in lateral and vertical dimensions
  - Materials Dependent
  - Subsequent Movement
  - Electrical Properties Highly Dependent upon Number and Distribution of Impurities
  - Diffusion at 800°C to 1200°C
- Source of Impurities
  - Deposition
  - Ion Implantation
    - Depth depending on ion speed/enery
    - More accurate control of doping levels
    - Fractures silicon crystaline structure during implant
    - Annealing occurs during diffusion
- Types of Impurities
  - n-type Arsenic, Antimony, Phosphorous
  - p-type Gallium, Aluminum, Boron

Diffusion



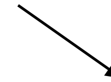
Before Diffusion



After Diffusion

Diffusion

Source of Impurities Implanted in Silicon Surface



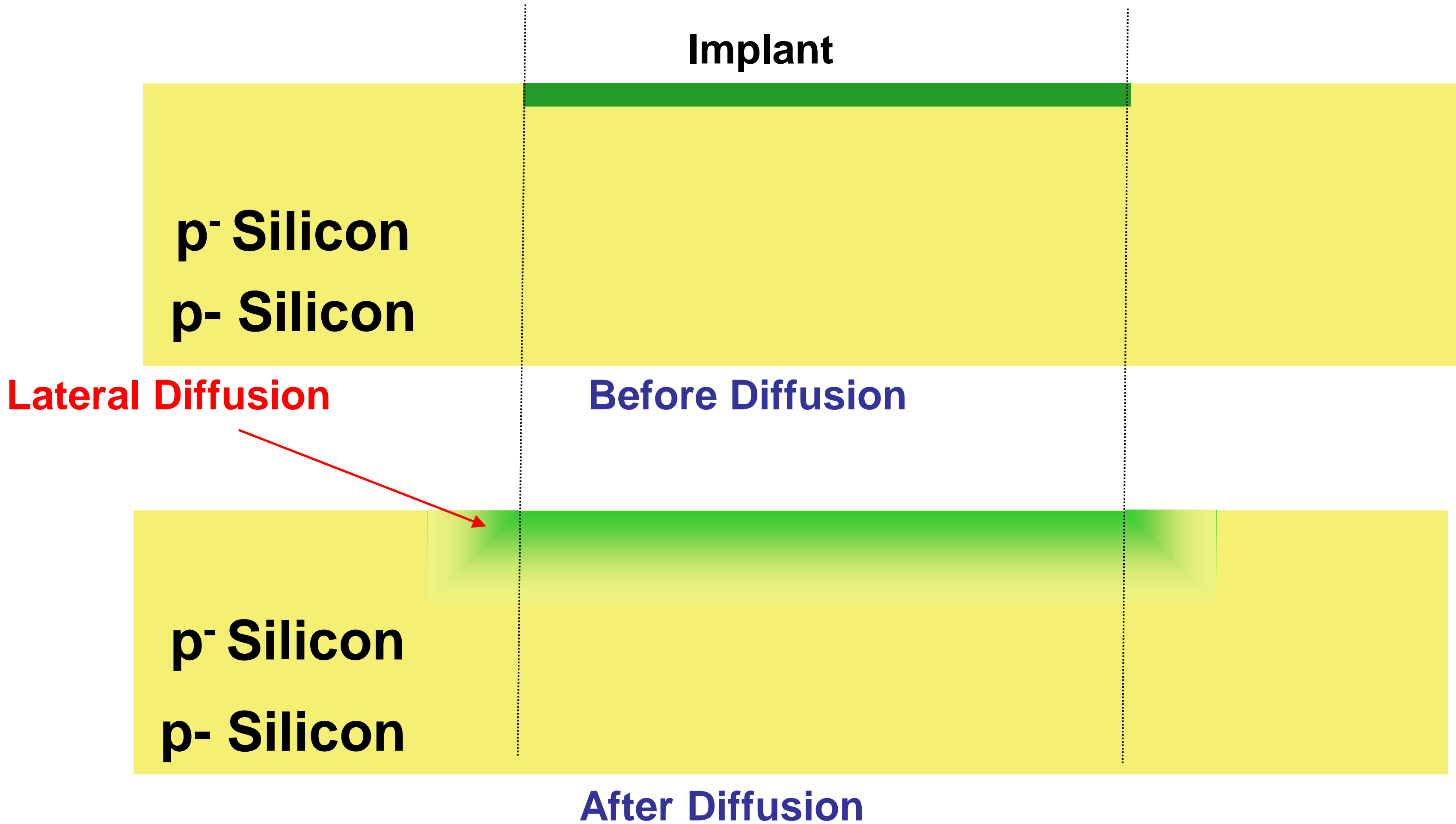
p$^-$ Silicon

Before Diffusion

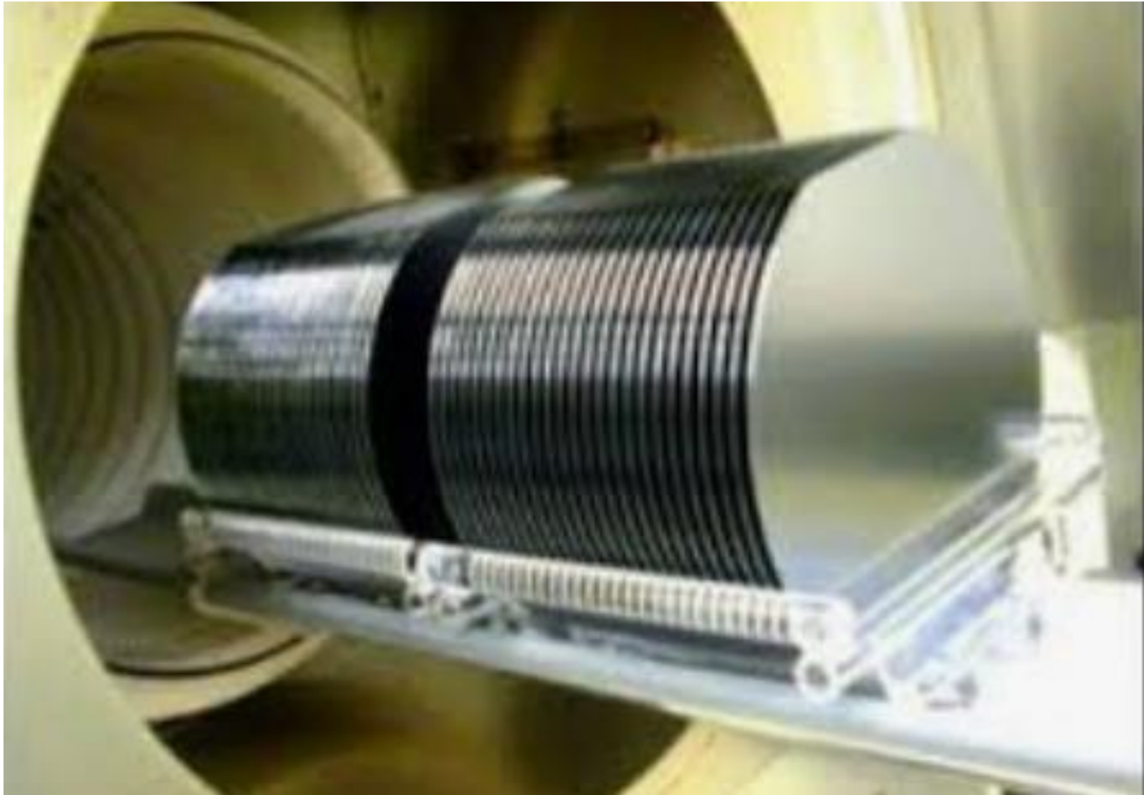
p$^-$ Silicon

After Diffusion

Diffusion

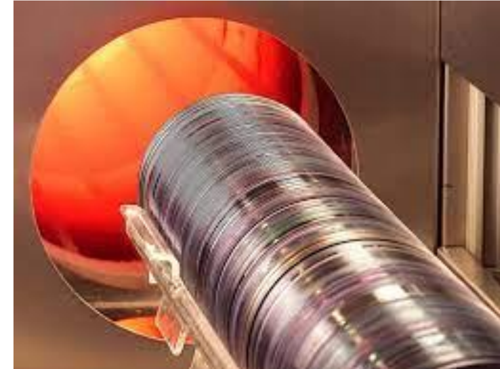


Diffusion



300mm wafers loading in diffusion furnace

Diffusion



Temperature for diffusion of impurities in silicon: $900^{o}C$ to $1100^{o}C$

Time, temperature, uniformity, and time-temperature profile strongly effect properties of semiconductor devices

Melting point of Silicon: $1420^{o}C$ (Poly around $1414^{o}C$)
Melting point of SiO_2: $1710^{o}C$
Melting point of Aluminum: $660^{o}C$
Melting point of Copper: $1085^{o}C$
Melting point of Quartz: $1670^{o}C$

Very approximately: diffusion rate targeted at 1um/hour
Very approximately: diffusion depths from 0.5um to 30um

Diffusion rate extremely low (but not 0) at normal operating temperatures

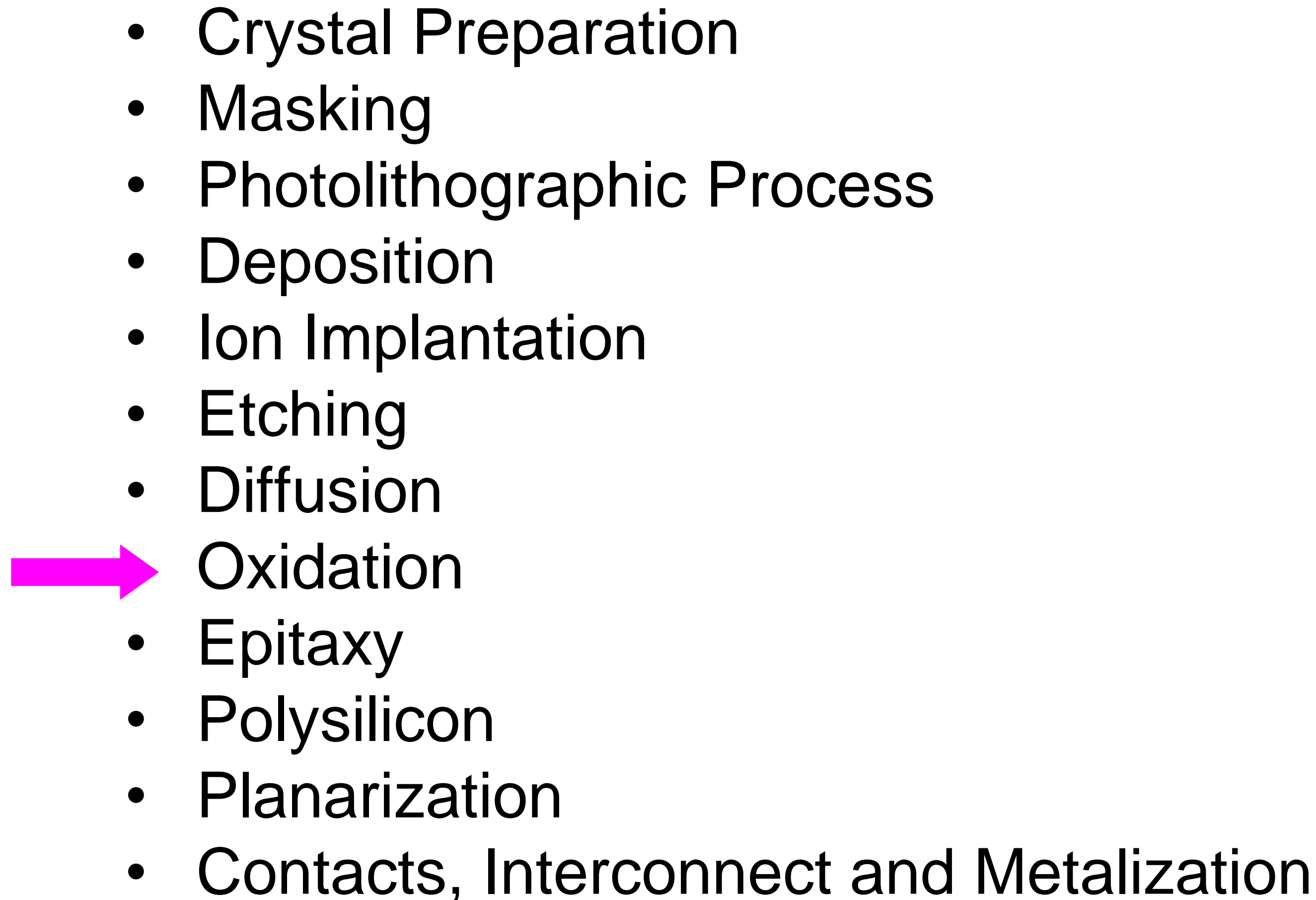
Student Question from Last Time

Why has Poly replaced Metal as the preferred gate material of MOS Transistors?

Part of the reason is associated with the melting temperature of Aluminum compared to Poly

This is associated with the goal of having processes with self-aligned gates (will be discussed later)

IC Fabrication Technology

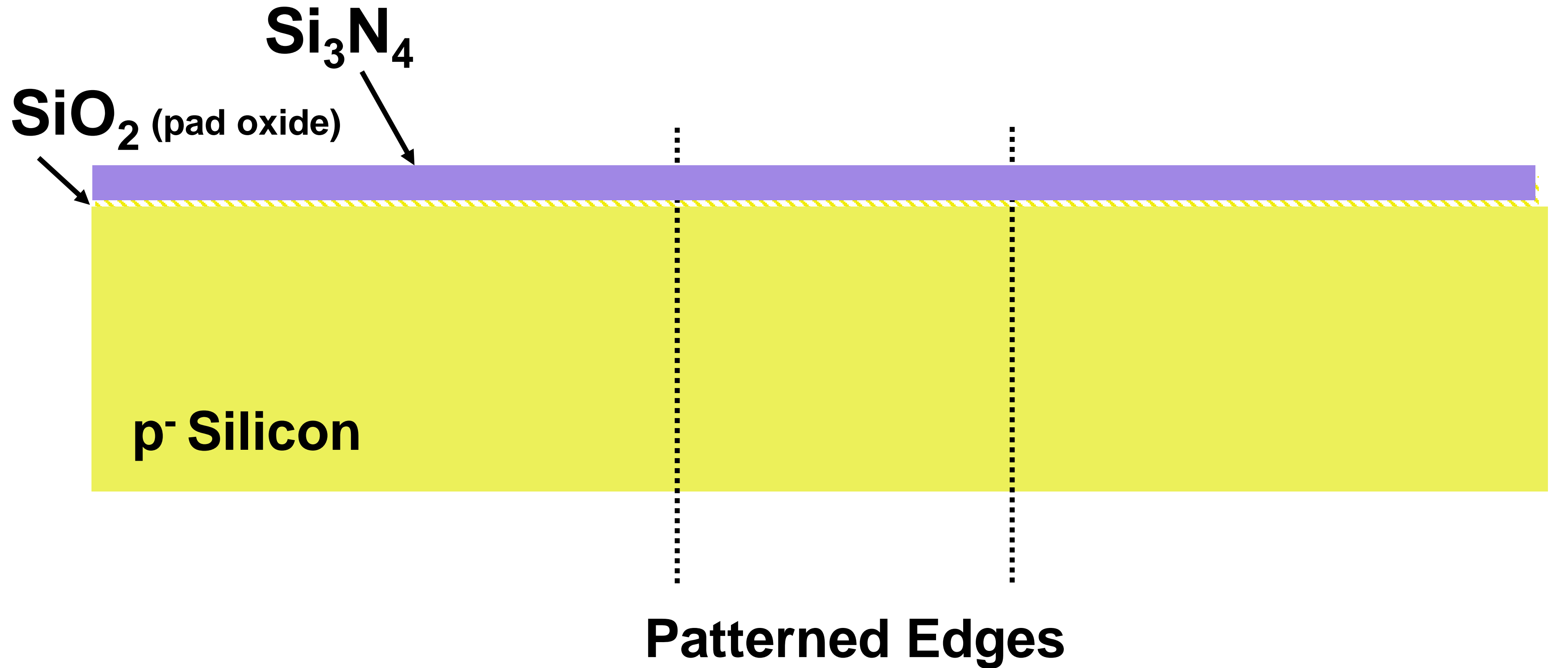


Oxidation

- SiO_2 is widely used as an insulator
  - Excellent insulator properties
- Used for gate dielectric
  - Gate oxide layers very thin
- Used to separate devices by raising threshold voltage
  - termed field oxide
  - field oxide layers very thick
- Methods of Oxidation
  - Thermal Growth (LOCOS)
    - Consumes host silicon
    - x units of SiO_2 consumes .47x units of Si
    - Undercutting of photoresist
    - Compromises planar surface for thick layers
    - Excellent quality
  - Chemical Vapor Deposition
    - Needed to put SiO_2 on materials other than Si

Oxidation

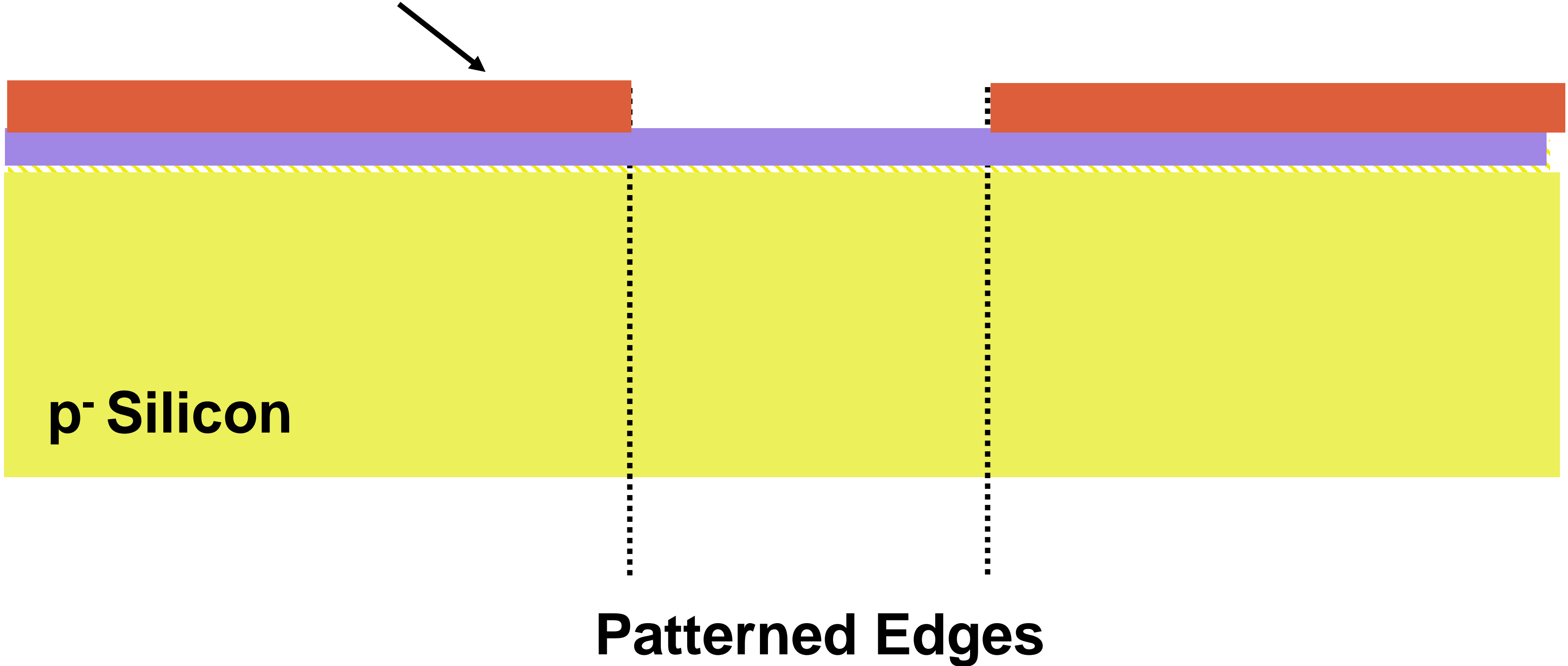
Thin layer of Silicon Nitride is deposited (serves as oxidation barrier)



Thermally Grown SiO_2 (LOCOS) - desired growth

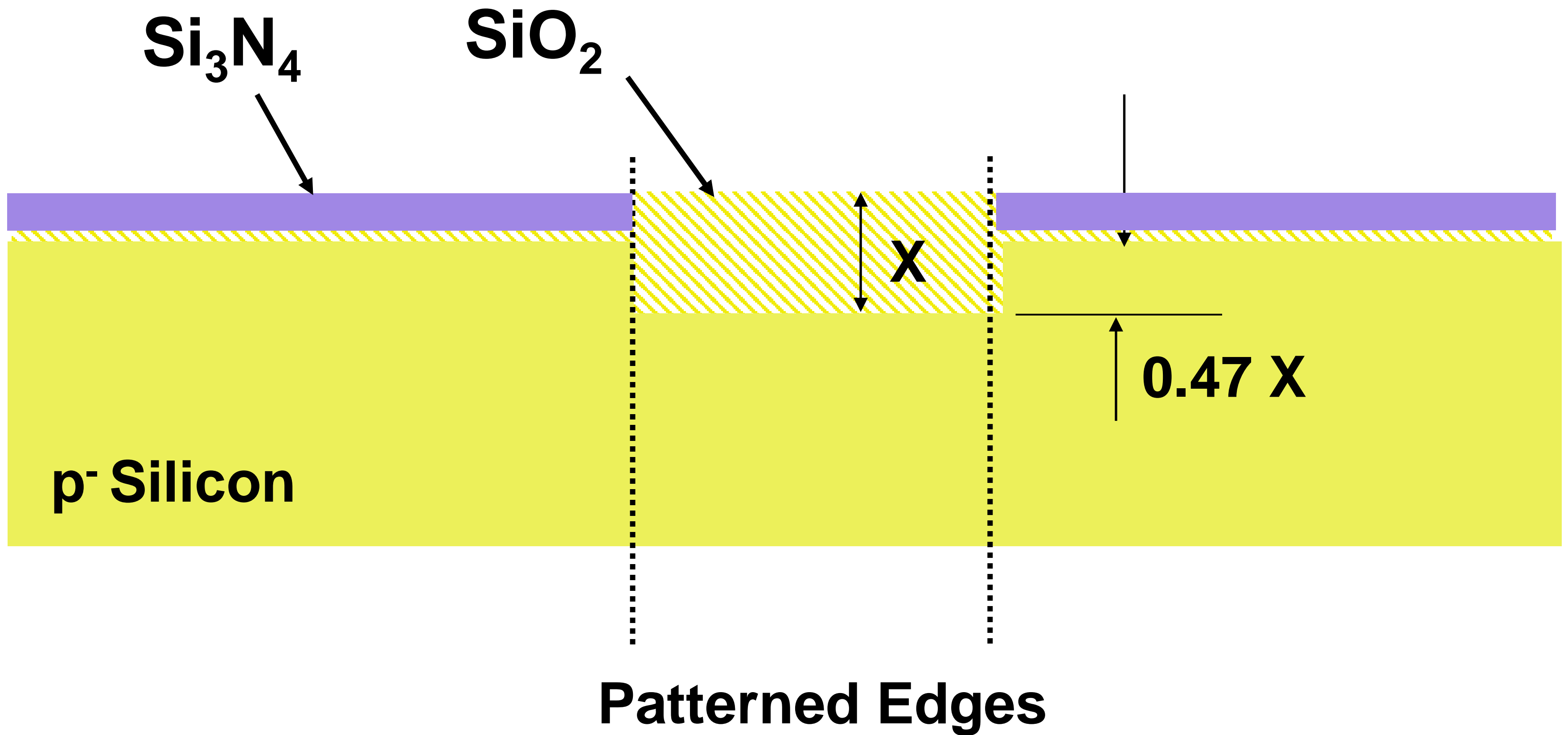
Oxidation

Silicon Nitride Patterned with Photoresist



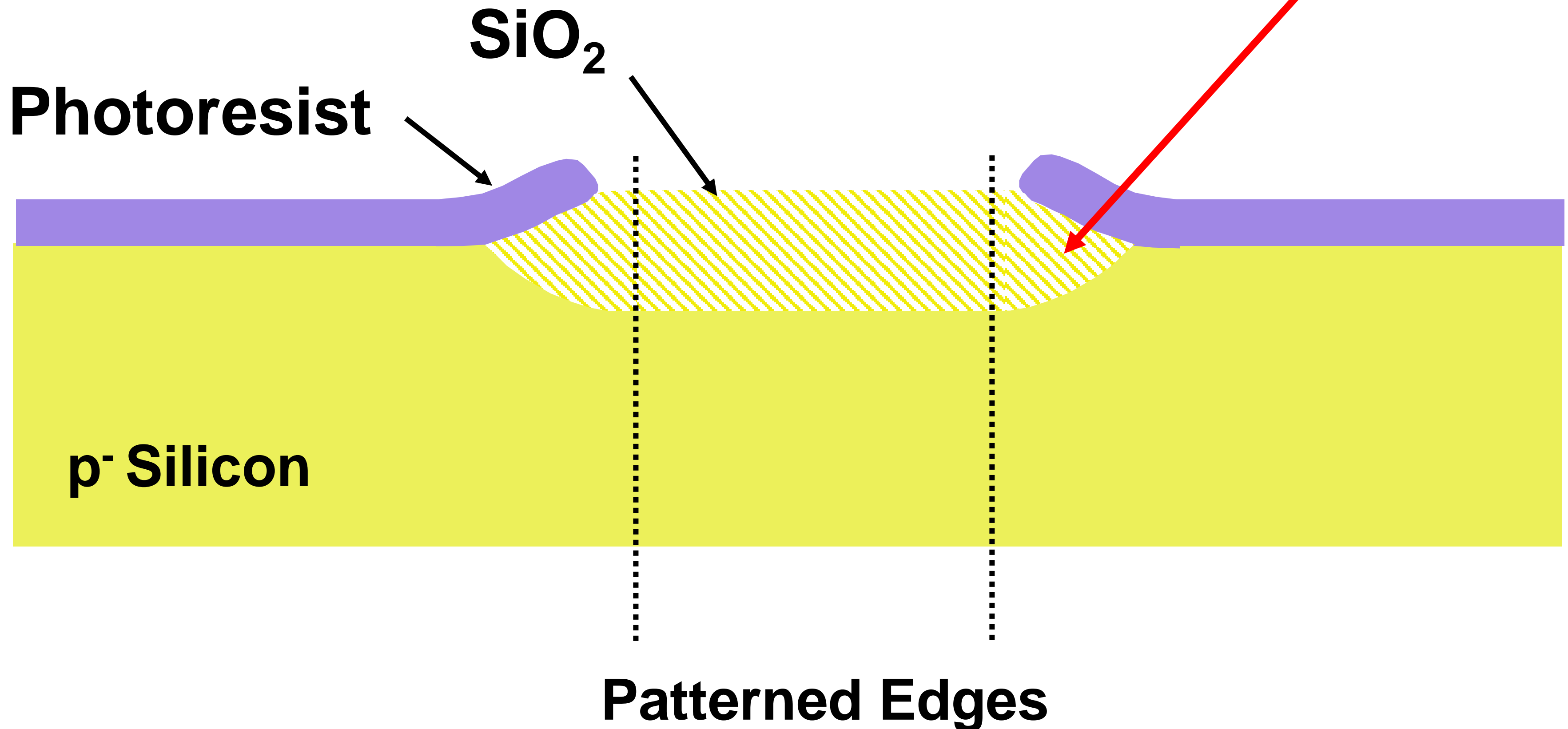
Thermally Grown SiO_2 - desired growth

Oxidation



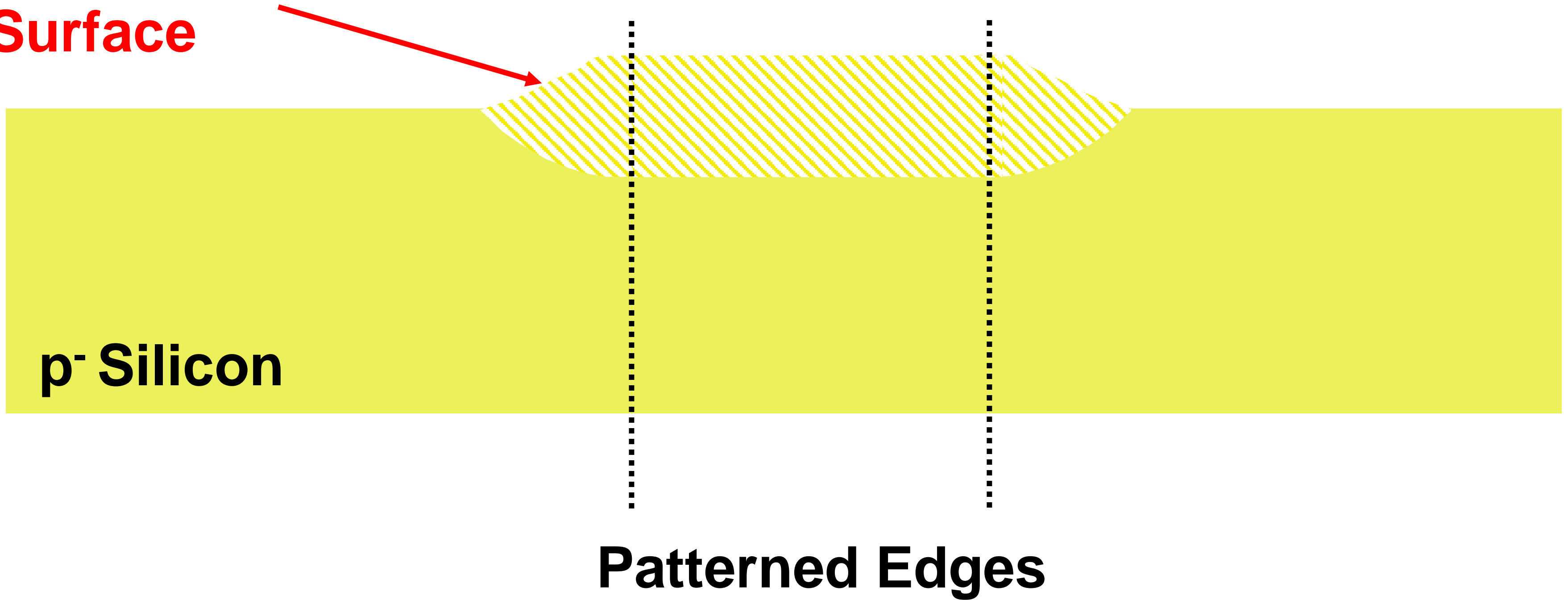
Thermally Grown SiO_2 - desired growth

Oxidation



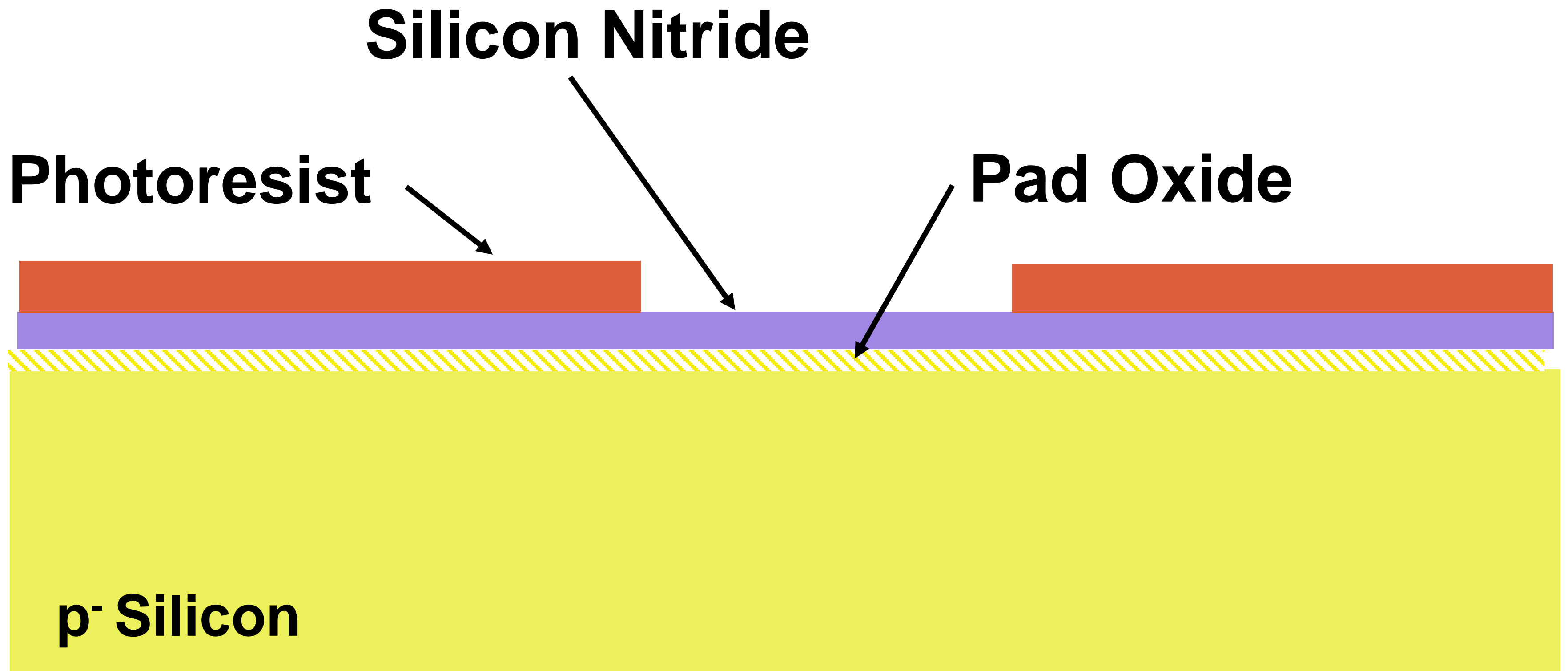
Thermally Grown SiO_2 - actual growth

Oxidation



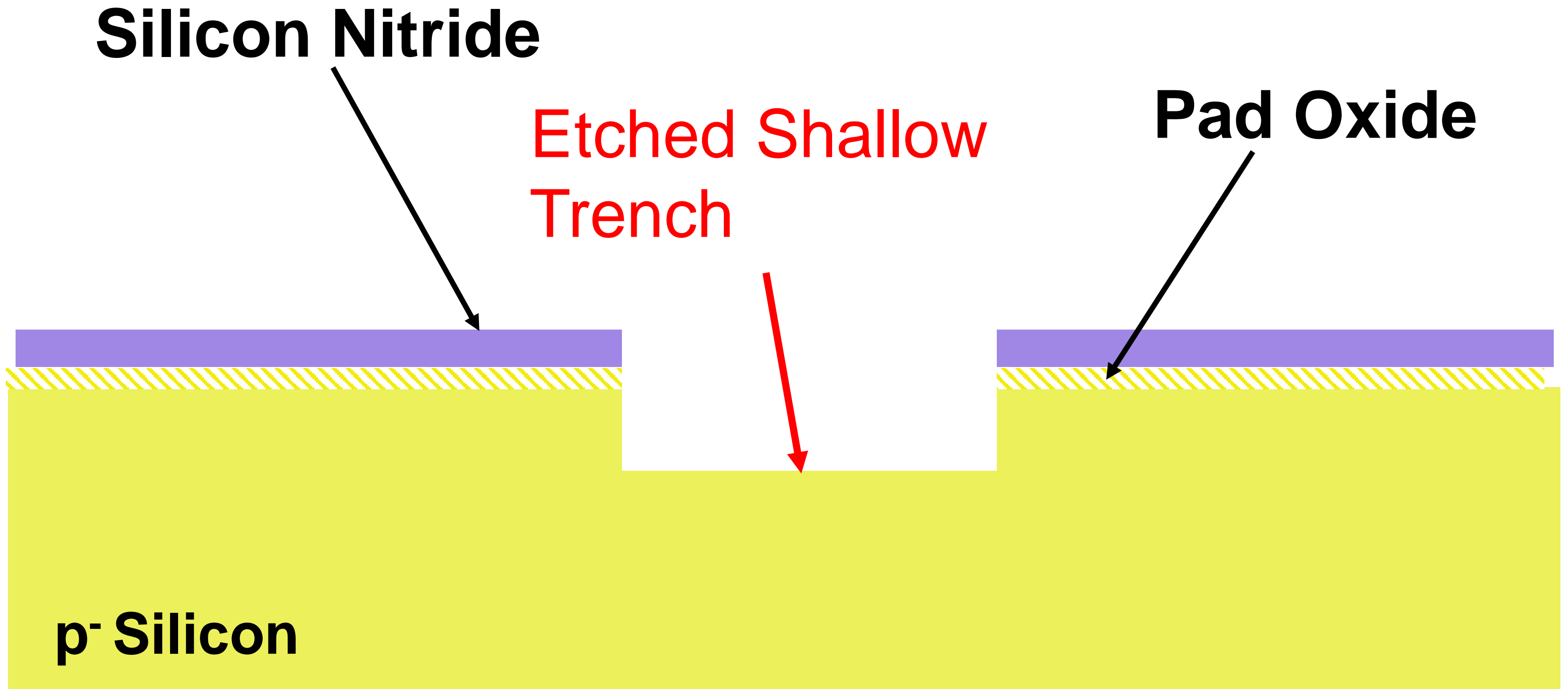
Thermally Grown SiO_2 - actual growth

Oxidation



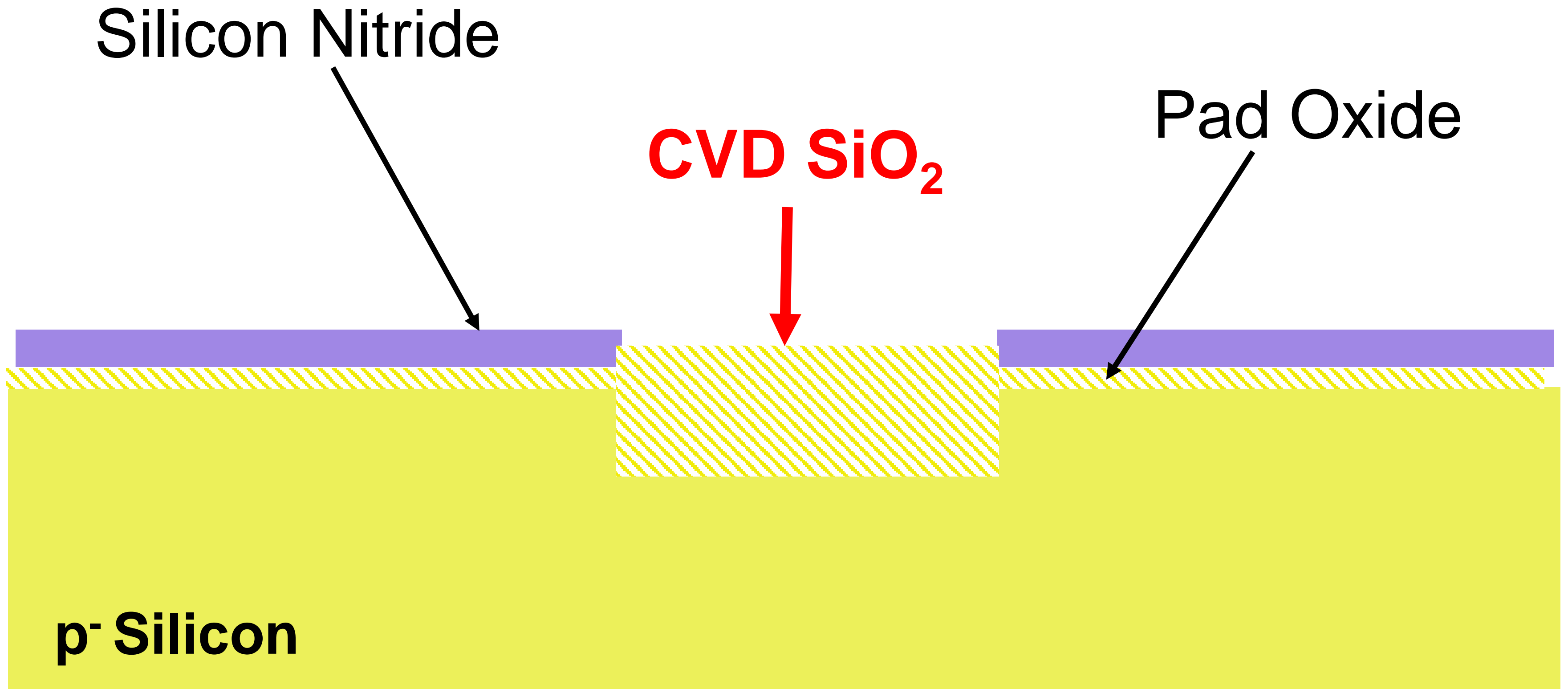
Shallow Trench Isolation (STI)

Oxidation



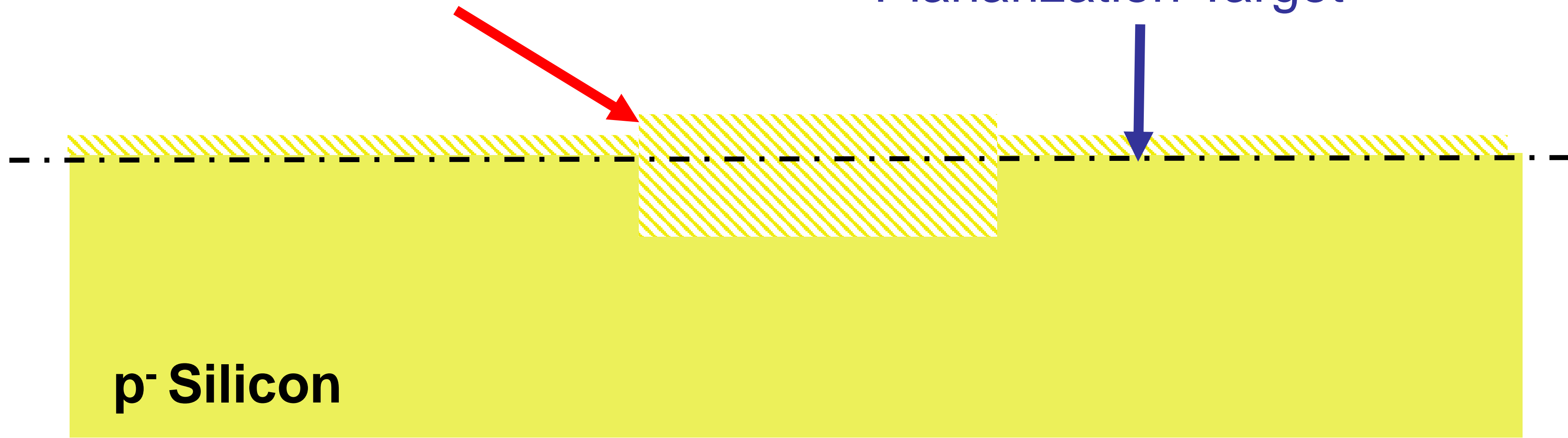
Shallow Trench Isolation (STI)

Oxidation



Shallow Trench Isolation (STI)

Oxidation



Shallow Trench Isolation (STI)

Oxidation

After Planarization

CVD SiO_2

Shallow Trench Isolation (STI)

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Epitaxy

- Single Crystaline Extension of Substrate Crystal
  - Commonly used in bipolar processes
  - CVD techniques
  - Impurities often added during growth
  - Grows slowly to allow alignmnt with substrate

Epitaxy

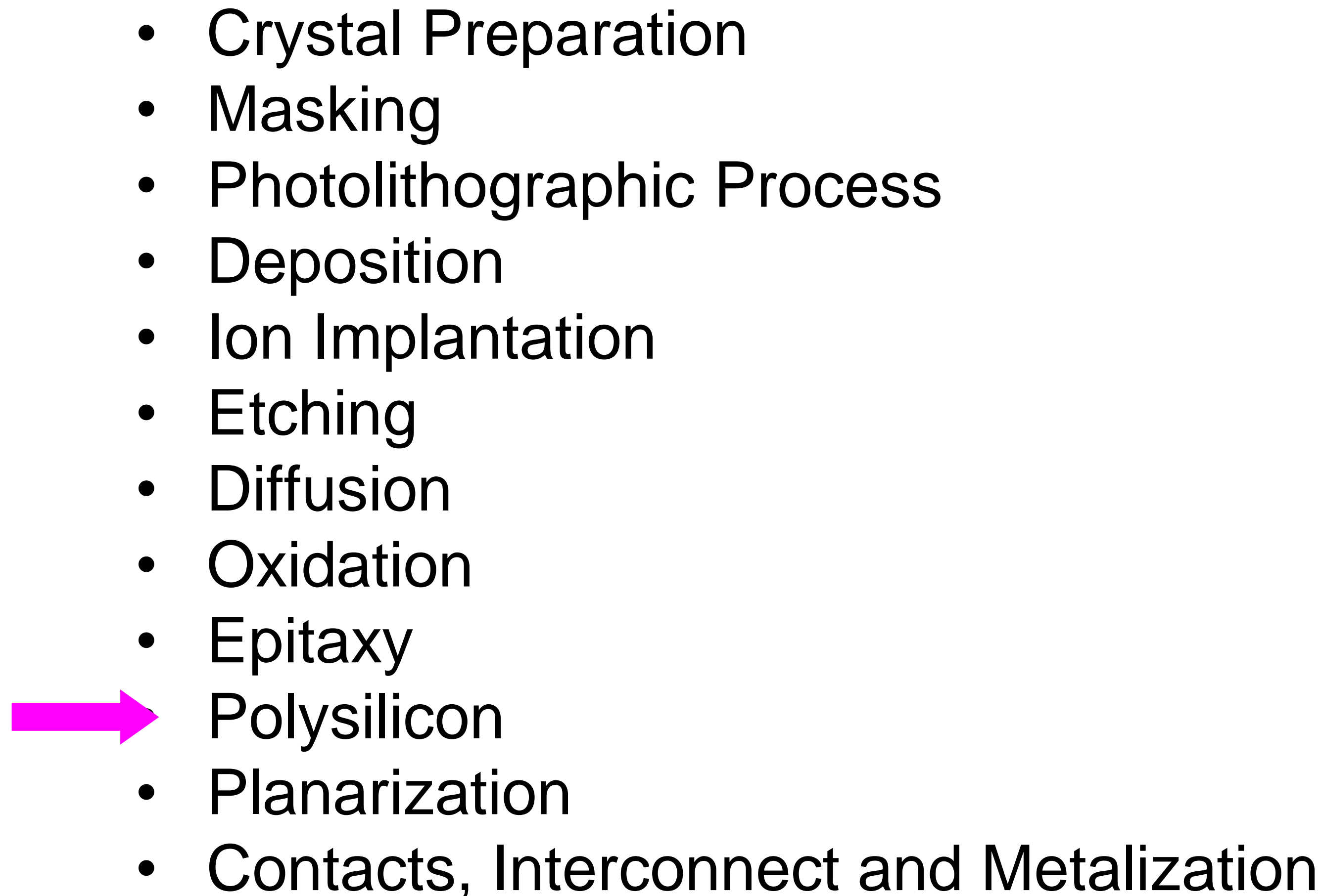
Epitaxial Layer

epi can be uniformly doped or graded

Original Silicon Surface

Question: Why can't a diffusion be used to create the same effect as an epi layer ?

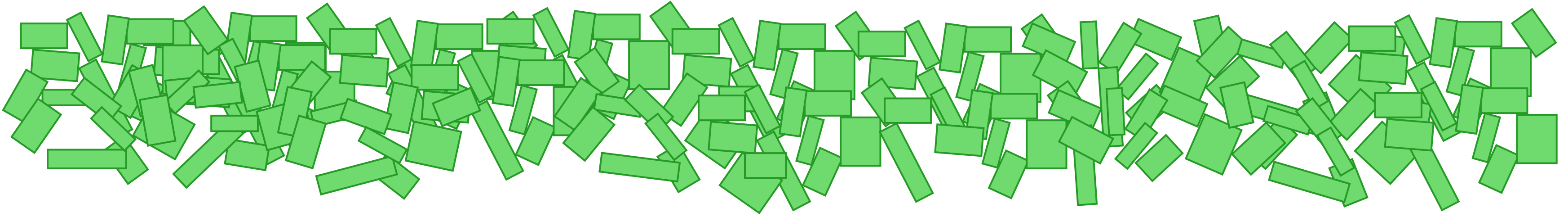
IC Fabrication Technology



Polysilicon

- Elemental contents identical to that of single crystaline silicon
  - Electrical properties much different
  - If doped heavily makes good conductor
  - If doped moderately makes good resistor
  - Widely used for gates of MOS devices
  - Widely used to form resistors
  - Grows fast over non-crystaline surface
  - Patterned with Photoresist/Etch process
  - Silicide often used in regions where resistance must be small
    - Refractory metal used to form silicide
    - Designer must indicate where silicide is applied (or blocked)

Polysilicon



Polysilicon

Single-Crystaline Silicon

Silicon Wafers and Solar Panels Made from Polysilicon

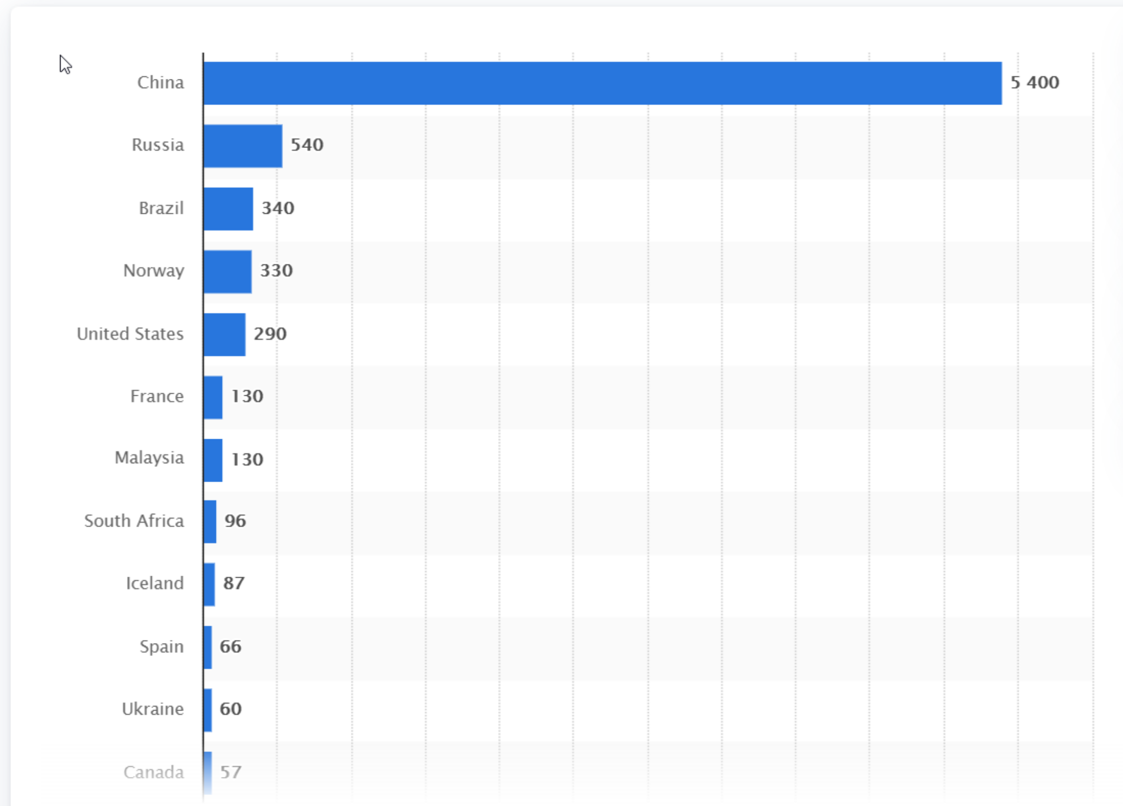
Where does the silicon come from?

In 2013:

Largest polysilicon producers in 2013 (market-share in %)			
GCL-Poly Energy	China	65,000 tons	22%
Wacker Chemie	Germany	52,000 tons	17%
OCI	South Korea	42,000 tons	14%
Hemlock Semiconductor	USA	36,000 tons	12%
REC	Norway	21,500 tons	7%

Source: Market Realist cites World production capacity at 300,000 tons in 2013.[2]
BNEF estimated actual production for 2013 at 227,000 tons[1]

In 2020:



In 2020:

The top 10 polysilicon manufacturers for 2020 include:

1. Tongwei (China)
2. Wacker (Germany/United States)
3. Daqo New Energy (China)
4. GCL-Poly (China)
5. Xinte Energy (China)
6. Xingjiang East Hope New Energy (China)
7. OCI (South Korea/Malaysia)
8. Asia Silicon (China)
9. Hemlock (United States)
10. Inner Mongolia Dongli Photovoltaic Electronics (China)

Top 4 projected to be from China by 2022

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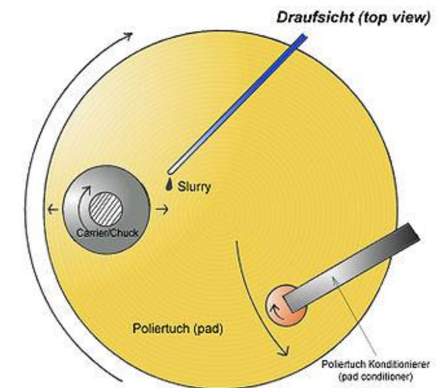
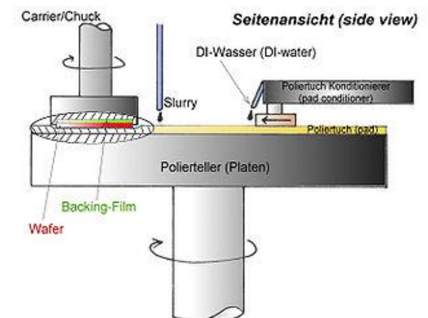
- Polysilicon
- ➡ Planarization
- Contacts, Interconnect and Metalization

Planarization

- Planarization used to keep surface planar during subsequent processing steps
  - Important for creating good quality layers in subsequent processing steps
  - Mechanically planarized





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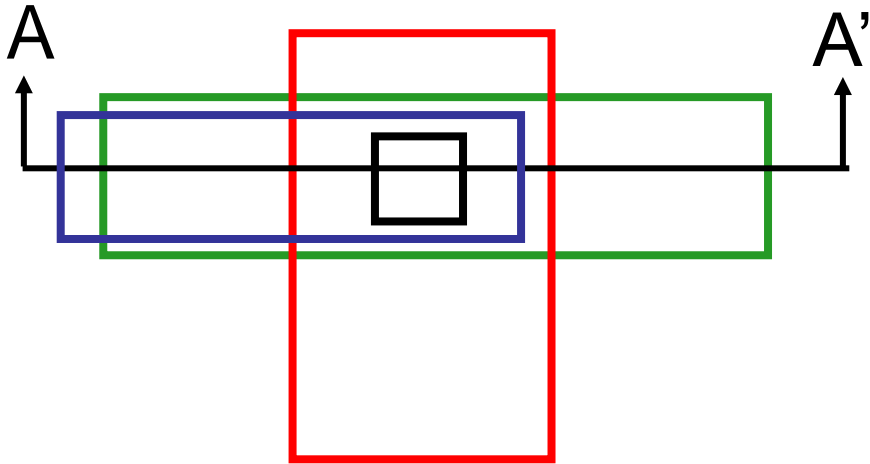
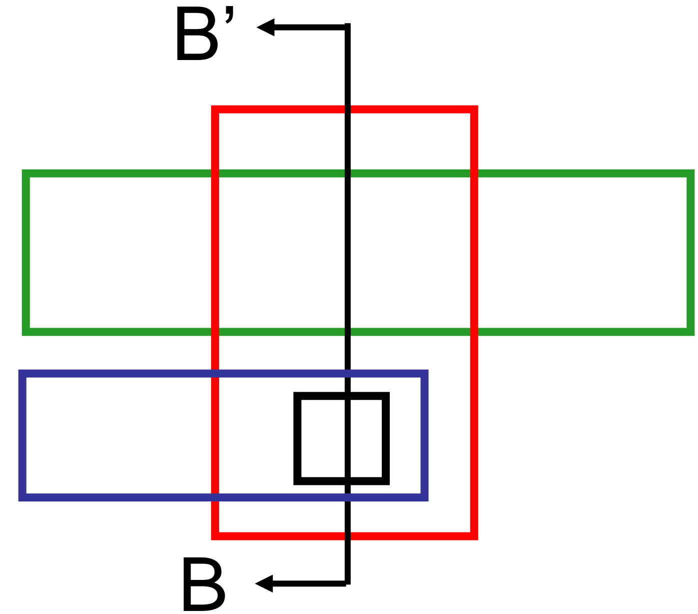
- → Contacts, Interconnect and Metalization

Contacts, Interconnect and Metalization

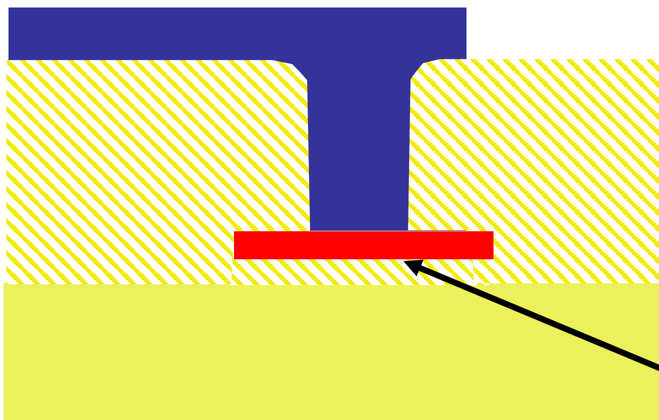
- Contacts usually of a fixed size
  - All etches reach bottom at about the same time
  - Multiple contacts widely used
  - Contacts not allowed to Poly on thin oxide in most processes
  - Dog-bone often needed for minimum-length devices

Contacts





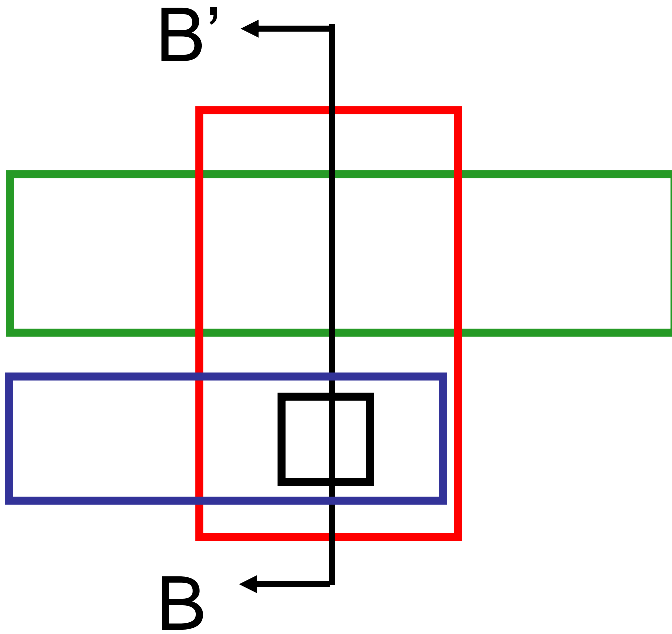
Acceptable Contact

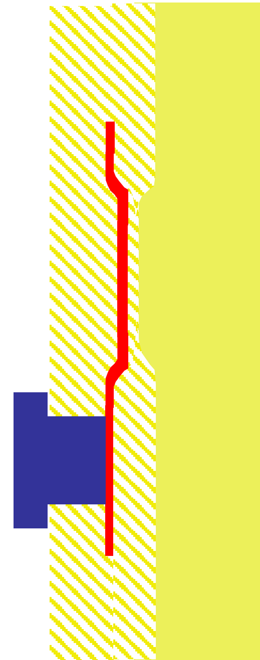


Unacceptable Contact

Vulnerable to pin holes
(usually all contacts are same size)

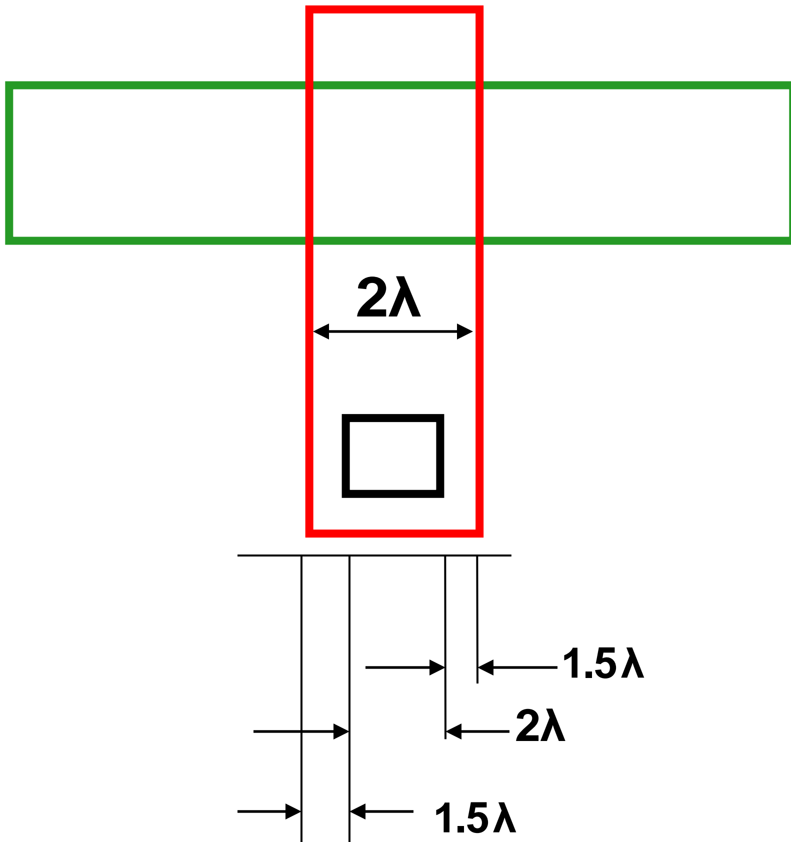
Contacts

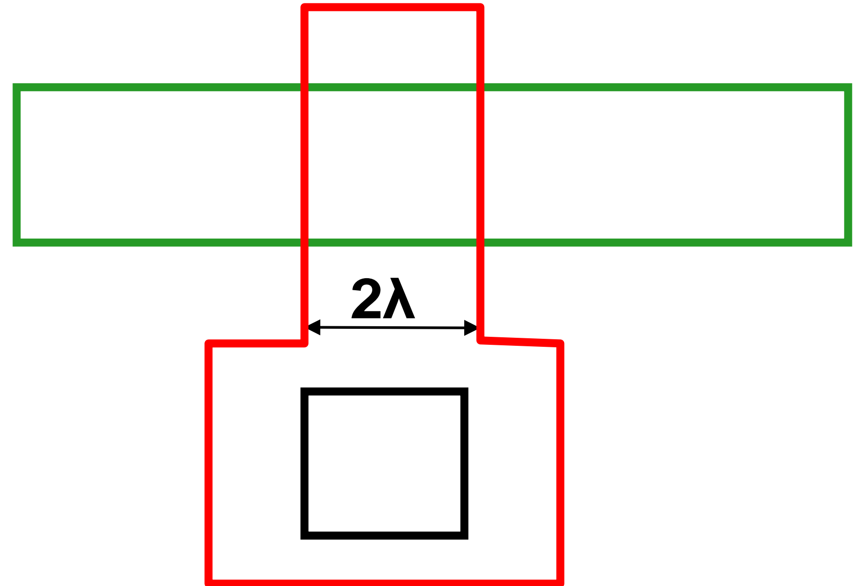




Acceptable Contact

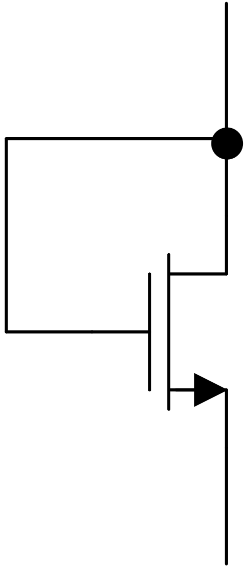
Contacts



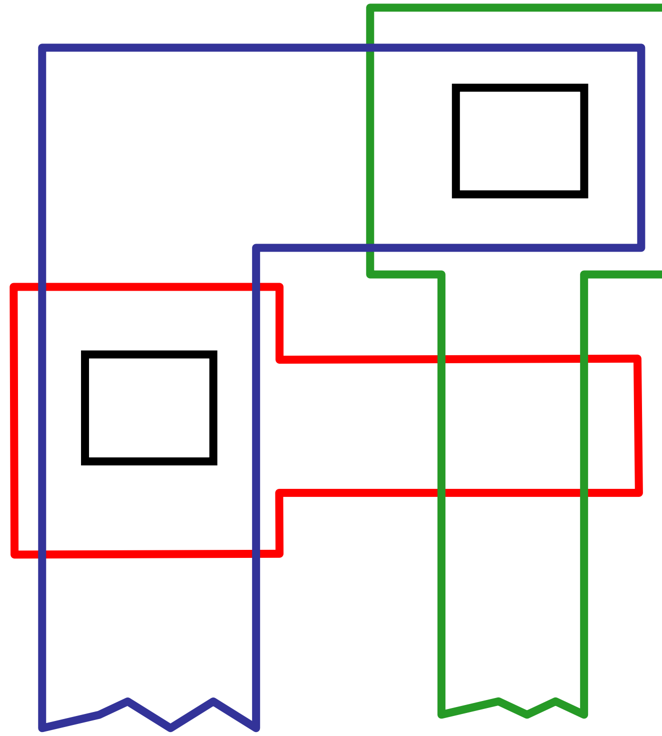


“Dog Bone” Contact

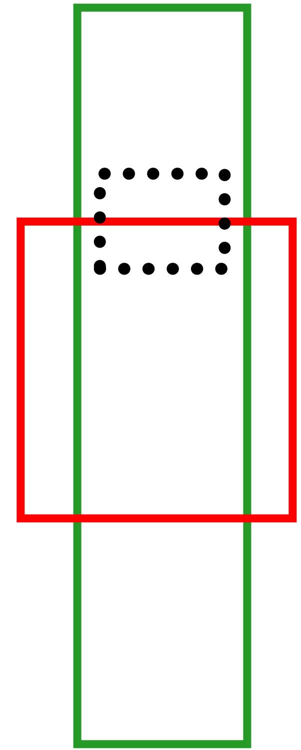
Contacts



Common
Circuit
Connection



Standard Interconnection



Buried Contact

Can save area but not
allowed in many processes

Metalization

- Aluminum widely used for interconnect
- Copper often replacing aluminum in recent processes
- Must not exceed maximum current density
  - around 1ma/u for aluminum and copper
- Ohmic Drop must be managed
- Parasitic Capacitances must be managed
- Interconnects from high to low level metals require connections to each level of metal
- Stacked vias permissible in some processes

Metalization

Aluminum

- Aluminum is usually deposited uniformly over entire surface and etched to remove unwanted aluminum
- Mask is used to define area in photoresist where aluminum is to be removed

Copper

- Plasma etches not effective at removing copper because of absence of volatile copper compounds
- Barrier metal layers needed to isolate silicon from migration of copper atoms
- Damascene or Dual-Damascene processes used to pattern copper

Stay Safe and Stay Healthy !

End of Lecture 10